SPECIFICATION
FOR
APPROVAL

(◆) **Preliminary Specification**
( ) **Final Specification**

Title	14.0” HD TFT LCD

Customer	
MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LP140WH6
Suffix	TJA1

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE
J. W Park / Manager	
REVIEWED BY	
N. D Son / Engineer	
PREPARED BY	
D. Y. Kim / Engineer S. W. Kim / Engineer	

Products Engineering Dept.
LG Display Co., Ltd

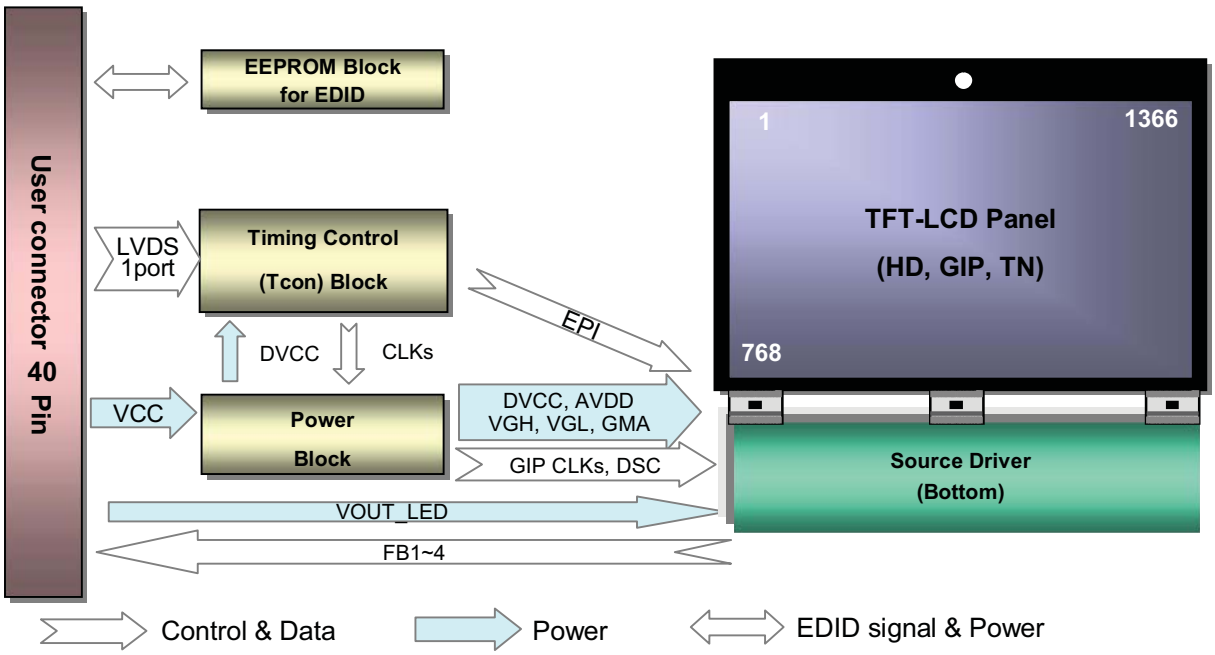
Contents

RECORD OF REVISIONS

Revision No	Revision Date	Page	Description	EDID ver
0.0	Nov.11. 2010	-	First Draft (Preliminary Specification)	
0.1	Jan.24. 2011	8	Add FPC CONNECTOR PIN CONFIGURATION	
		14	Add Recommend Power Sequence	
		23	Add Inspection Free Area	
0.2	Feb.14. 2011	19	Update Mechanical Characteristics	
0.3	Mar.10. 2011	6-7	Update Electrical Specifications	
		12	Update Signal Timing Specifications	
		16	Update Optical Specification	
		20-21	Update drawing	
		23	Update packing	
		26-28	Update Inspection Free Area / Panel Burr & Chip	
		29	Add Web-Cam Hole Shift	
0.4	Mar.16. 2011	4	Update Transmittance and Power Consumption	
		6	Update Power Consumption	
		16	Update Transmittance and fclk	
		30-32	Update EDID	1.0
0.5	Mar.22. 2011	29	Update Web-Cam Hole Shift	

1. General Description

The LP140WH6 is a Color Active Matrix Liquid Crystal Display. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally white mode. This TFT-LCD has 14.0 inches diagonally measured active display area with HD resolution (1366 horizontal by 768 vertical pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 6-bit gray scale signal for each dot, thus, presenting a palette of more than 262,144 colors. The LP140WH6 has been designed to apply the interface method that enables low power, high speed, low EMI. The LP140WH6 is intended to support applications where thin thickness, low power are critical factors and graphic displays are important. In combination with the vertical arrangement of the sub-pixels, the LP140WH6 characteristics provide an excellent flat display for office automation products such as Notebook PC.



General Features

Active Screen Size	14.0 inches diagonal
Outline Dimension	1) Panel (W/O PCB) : 322.0(H, Typ.) × 198.68(V, Typ.) [mm] 2) Panel (With PCB) : 322.0(H, Typ.) × 211.18(V, Typ.) [mm]
Pixel Pitch	0.2265mm × 0.2265 mm
Pixel Format	1366 horiz. by 768 vert. Pixels RGB strip arrangement
Color Depth	6-bit, 262,144 colors
Transmittance (With POL)	6.1% (Typ.)
Power Consumption	Logic : 0.9W (Typ.@ Mosaic)
Weight	190 g (Max.)
Display Operating Mode	Transmissive mode, normally white
Surface Treatment	Glare treatment (3H) of the front Polarizer
RoHS Compliance	Yes
BFR / PVC / As Free	Yes for all

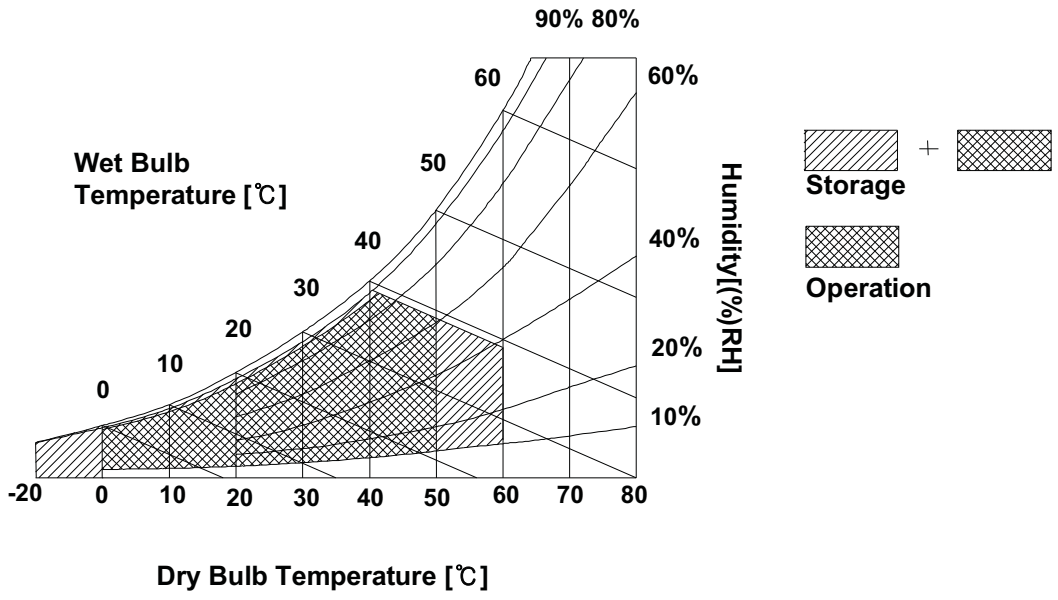
2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Values		Units	Notes
		Min	Max		
Power Input Voltage	VCC	-0.3	4.0	Vdc	at 25 ± 5°C
Operating Temperature	TOP	0	50	°C	1
Storage Temperature	HST	-20	60	°C	1
Operating Ambient Humidity	HOP	10	90	%RH	1
Storage Humidity	HST	10	90	%RH	1

Note : 1. Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39°C Max, and no condensation of water.



3. Electrical Specifications

3-1. Electrical Characteristics

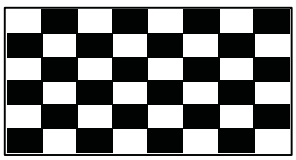
The LP140WH6 requires one power inputs. The first logic is employed to power the LCD electronics and to drive the TFT array and liquid crystal.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Values			Unit	Notes
			Min	Typ	Max		
LOGIC :							
Power Supply Input Voltage		V_{CC}	3.0	3.3	3.6	V	1
Power Supply Input Current	Mosaic	I_{CC}	227	268	333	mA	2
Power Consumption	Mosaic	P_{CC}	-	0.9	1.1	W	2
Power Supply Inrush Current		I_{CC_P}	-	-	1500	mA	3
LVDS Impedance		Z_{LVDS}	90	100	110	Ω	4
LED : W/O LED Driver, 4string x 9ea							
LED Output Voltage		V_{OUT}		28.8	30.6	V	
LED Output Current		I_{OUT}		76	78	mA	
LED Power Consumption	Full Duty	P_{OUT}		2.2	2.39	W	

Note)

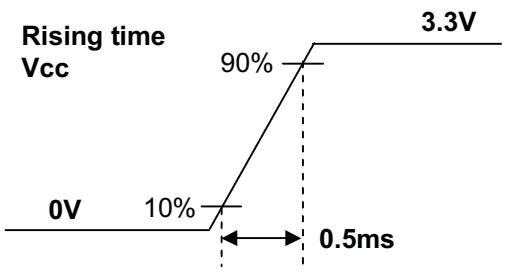
1. The measuring position is the connector of Board Ass'y and the test conditions are under 25℃, fv = 60Hz, Black pattern.
2. The specified Icc current and power consumption are under the Vcc = 3.3V , 25℃, fv = 60Hz condition.
3. This Spec. is the max load condition for the cable impedance designing.

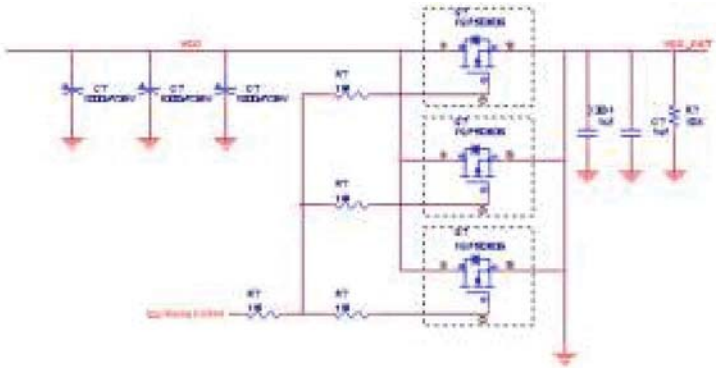


Mosaic Pattern

4. This impedance value is needed for proper display and measured form LVDS Tx to the mating connector.

** The below figures are the measuring Vcc condition and the Vcc control block LGD used.
The Vcc condition is same as the minimum of T1 at Power on sequence.

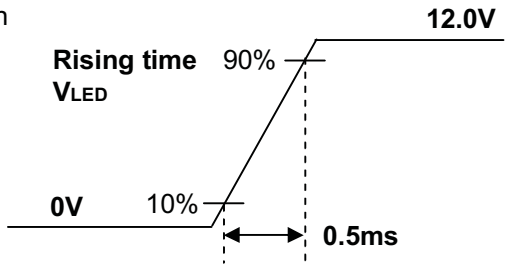




※ LGD recommend below Electrical Characteristics of LED Driver.

Parameter	Symbol	Values			Unit	Notes
		Min	Typ	Max		
BACKLIGHT : (with LED Driver)						
LED Power Inrush Current	I_{LED_P}	-	500	1000	mA	7
PWM Duty Ratio		1	-	100	%	8
PWM Jitter	-	0	-	0.2	%	9
PWM Impedance	Z_{PWM}	20	40	60	kΩ	
PWM Frequency	F_{PWM}	200	-	1000	Hz	10
PWM High Level Voltage	V_{PWM_H}	2.2	-	5.3	V	
PWM Low Level Voltage	V_{PWM_L}	0	-	0.3	V	
LED_EN Impedance	Z_{PWM}	20	40	60	kΩ	
LED_EN High Voltage	$V_{LED\_EN\_H}$	2.2	-	5.3	V	
LED_EN Low Voltage	$V_{LED\_EN\_L}$	0	-	0.3	V	

7. The current and power consumption with LED Driver are under the Vled = 12.0V , 25℃, Dimming of Max luminance and White pattern with the normal frame frequency operated(60Hz).
8. The below figures are the measuring Vled condition and the Vled control block LGD used.
   VLED control block is same with Vcc control block.



9. The operation of LED Driver below minimum dimming ratio may cause flickering or reliability issue. If Jitter of PWM is bigger than maximum, it may induce flickering.
10. This Spec. is not effective at 100% dimming ratio as an exception because it has DC level equivalent to 0Hz. In spite of acceptable range as defined, the PWM Frequency should be fixed and stable for more consistent brightness control at any specific level desired.

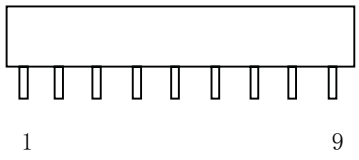
3-2. Interface Connections

This Board Ass'y employs two interface connections, a 40 pin connector used for the module electronics interface and the other connector used for the integral backlight system.

Table 3. MODULE CONNECTOR PIN CONFIGURATION (CN1)

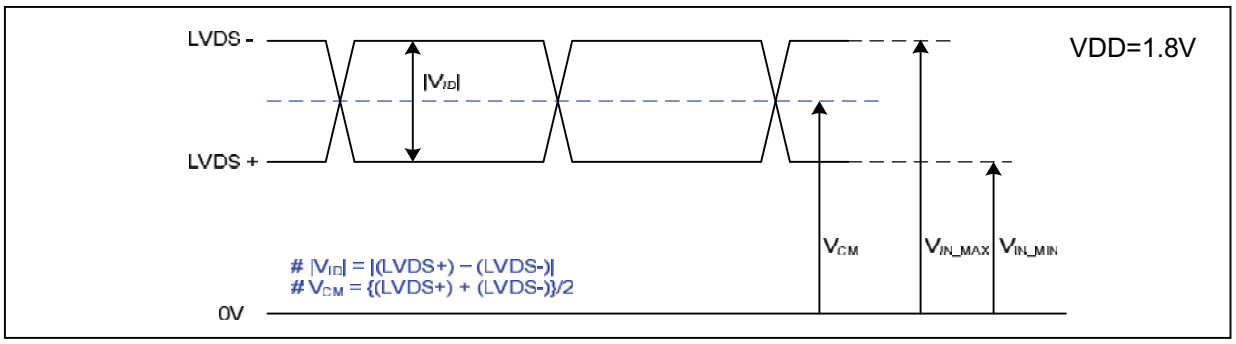
Pin	Symbol	Description	Notes
1	NC	No Connection	**[Interface Chip]** 1. LCD : **TLi, TL2343EP (LCD Controller)** Including LVDS Receiver. . 2. System : LVDSRx or equivalent * Pin to Pin compatible with LVDS **[Connector]** JAE HD1S040HA1 LSMtron GT05Q-40S-H10 or equivalent **[Mating Connector]** 20345-#40E-## series or equivalent **[LED Block]** LED block move to system set base **[Connector pin arrangement]** Check B/Ass'y drawing (Page 20)
2	VCC	LCD Logic and driver power (3.3V Typ.)	
3	VCC	LCD Logic and driver power (3.3V Typ.)	
4	V EEDID	DDC Power (3.3V)	
5	BIST	BIST	
6	Clk EEDID	DDC Clock	
7	DATA EEDID	DDC Data	
8	ORX0-	Negative LVDS differential data input	
9	ORX0+	Positive LVDS differential data input	
10	GND	LCM Ground	
11	ORX1-	Negative LVDS differential data input	
12	ORX1+	Positive LVDS differential data input	
13	GND	LCM Ground	
14	ORX2-	Negative LVDS differential data input	
15	ORX2+	Positive LVDS differential data input	
16	GND	LCM Ground	
17	ORXC-	Negative LVDS differential clock input	
18	ORXC+	Positive LVDS differential clock input	
19	NC	No Connection	
20	NC	No Connection	
21	NC	No Connection	
22	GND	LCM Ground	
23	NC	No Connection	
24	NC	No Connection	
25	GND	LCM Ground	
26	NC	No Connection	
27	NC	No Connection	
28	GND	LCM Ground	
29	NC	No Connection	
30	NC	No Connection	
31	FB4	Regulated Current sink	
32	FB3	Regulated Current sink	
33	FB2	Regulated Current sink	
34	FB1	Regulated Current sink	
35	NC	No Connection	
36	NC	No Connection	
37	NC	No Connection	
38	VOUT	Boost output voltage	
39	VOUT	Boost output voltage	
40	VOUT	Boost output voltage	

Table 3-1. FPC CONNECTOR PIN CONFIGURATION (CN2)

Pin	Symbol	Description	Notes
1	VOUT_LED	LED Anode(Positive)	
2	FB1	LED Cathode (Negative)	
3	VOUT_LED	LED Anode(Positive)	
4	FB2	LED Cathode (Negative)	
5	VOUT_LED	LED Anode(Positive)	
6	FB3	LED Cathode (Negative)	
7	VOUT_LED	LED Anode(Positive)	
8	FB4	LED Cathode (Negative)	
9	N.C	No Connection	

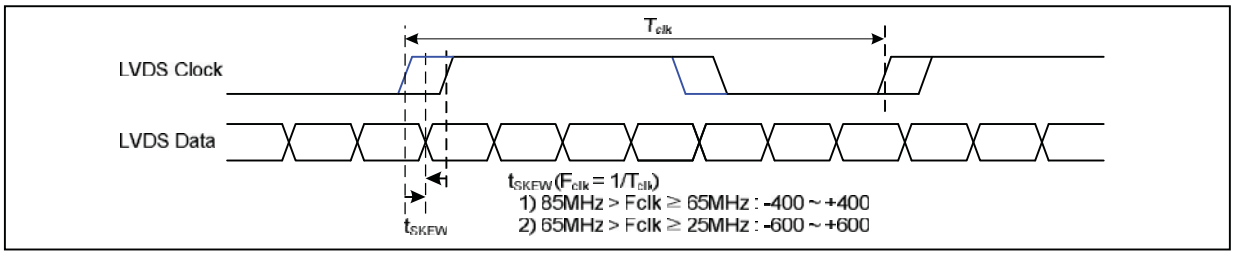
3-3. LVDS Signal Timing Specifications

3-3-1. DC Specification

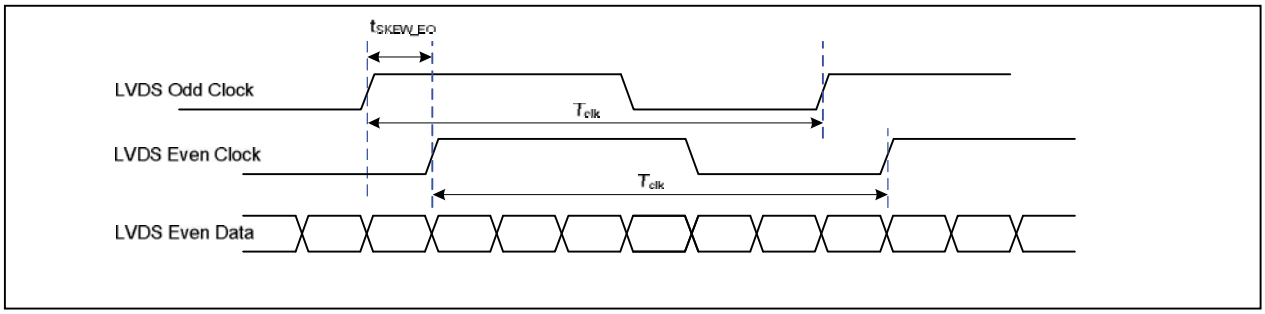


Description	Symbol	Min	Typ	Max	Unit	Notes
LVDS Differential Voltage	$\|V_{ID}\|$	100	-	600	mV	-
LVDS Common mode Voltage	V_{CM}	$\|V_{ID}\|$ /2	1.2	VDD- $\|V_{ID}\|$/2	V	-
LVDS Input Voltage Range	V_{IN}	0.3	-	VDD	V	-

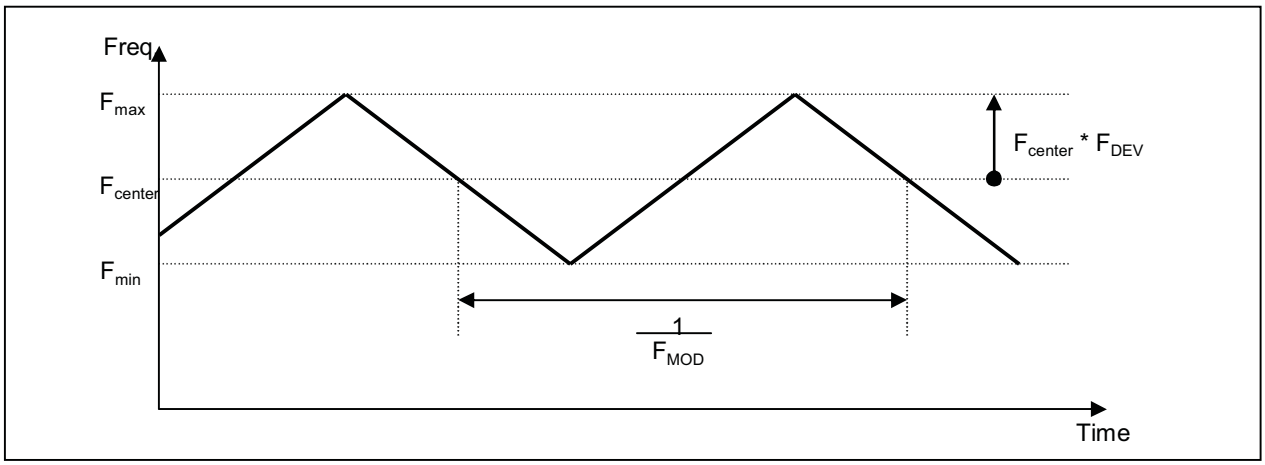
3-3-2. AC Specification



Description	Symbol	Min	Max	Unit	Notes
LVDS Clock to Data Skew Margin	t_{SKEW}	- 400	+ 400	ps	85MHz > Fclk ≥ 65MHz
	t_{SKEW}	- 600	+ 600	ps	65MHz > Fclk ≥ 25MHz
LVDS Clock to Clock Skew Margin (Even to Odd)	t_{SKEW_EO}	- 1/7	+ 1/7	T_{clk}	-
Maximum deviation of input clock frequency during SSC	F_{DEV}	-	± 3	%	-
Maximum modulation frequency of input clock during SSC	F_{MOD}	-	200	KHz	-



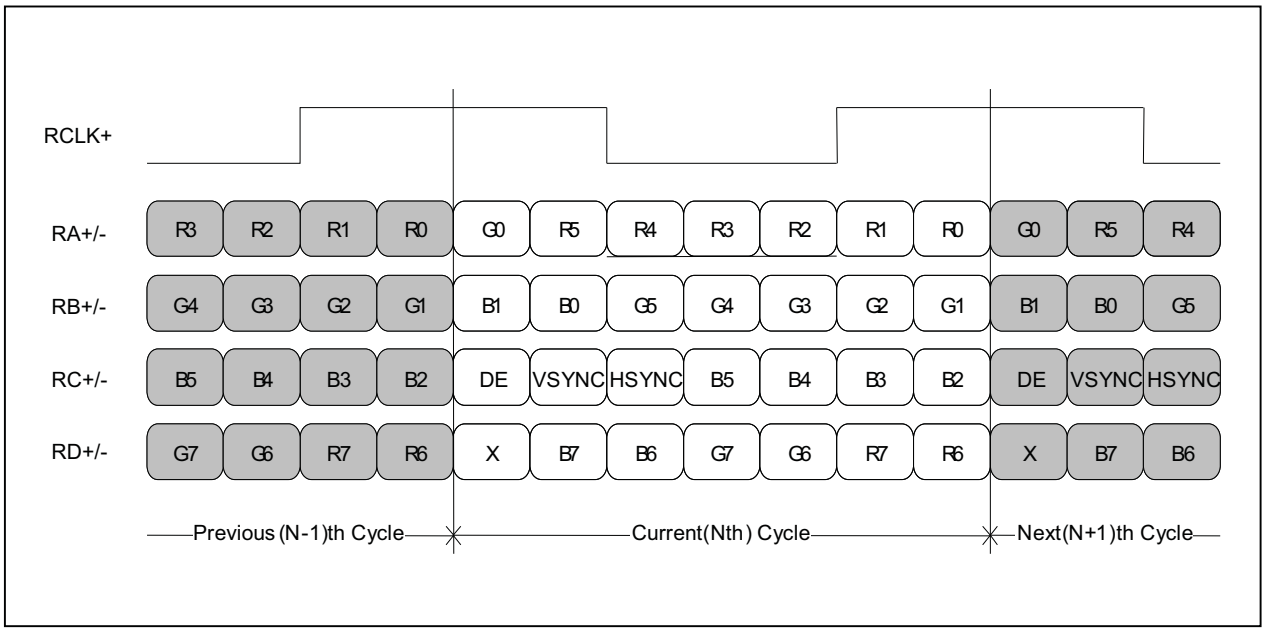
< Clock skew margin between channel >



< Spread Spectrum >

3-3-3. Data Format

1) LVDS 1 Port



< LVDS Data Format >

3-4. Signal Timing Specifications

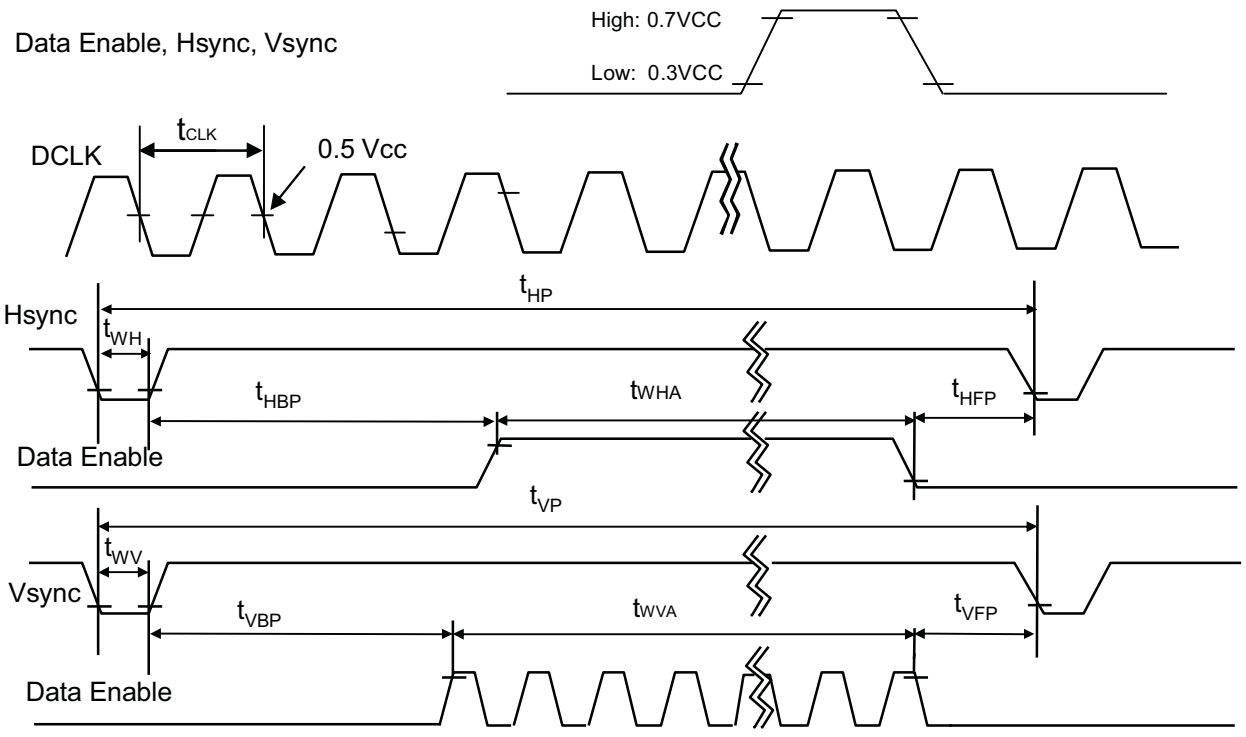
This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications and specifications of LVDS Tx/Rx for its proper operation.

Table 4. TIMING TABLE

ITEM	Symbol		Min	Typ	Max	Unit	Note
DCLK	Frequency	f_{CLK}	68.1	70.0	73.0	MHz	
Hsync	Period	t_{HP}	1462	1492	1536	tCLK	
	Width	t_{WH}	32	48	62		
	Width-Active	t_{WHA}	1366	1366	1366		
Vsync	Period	t_{VP}	776	782	792	tHP	
	Width	t_{WV}	2	5	8		
	Width-Active	t_{WVA}	768	768	768		
Data Enable	Horizontal back porch	t_{HBP}	34	42	60	tCLK	
	Horizontal front porch	t_{HFP}	32	36	40		
	Vertical back porch	t_{VBP}	4	6	12	tHP	
	Vertical front porch	t_{VFP}	2	3	4		

3-5. Signal Timing Waveforms

Condition : VCC =3.3V



3-6. Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color ; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 5. COLOR DATA REFERENCE

Color		Input Color Data																	
		RED						GREEN						BLUE					
		MSB					LSB	MSB					LSB	MSB					LSB
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	...			...						...						...			
	RED (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	...			...						...						...			
	GREEN (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	GREEN (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
BLUE	BLUE (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	...			...						...						...			
	BLUE (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	BLUE (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

3-7. Power Sequence

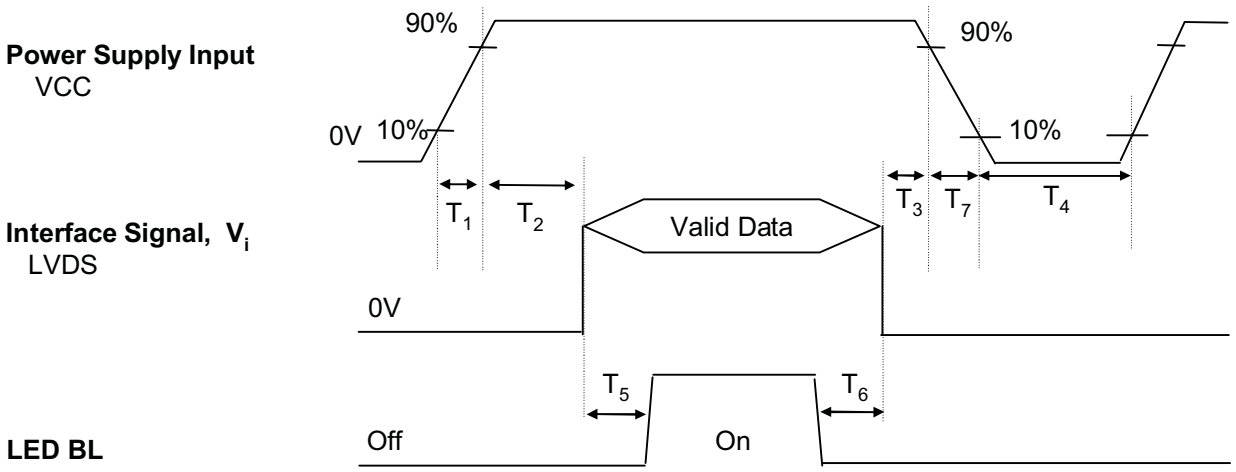


Table 6. POWER SEQUENCE TABLE

Logic Parameter	Value			Units
	Min.	Typ.	Max.	
T_1	0.5	-	10	ms
T_2	0	-	50	ms
T_3	0	-	50	ms
T_4	400	-	-	ms
T_5	200	-	-	ms
T_6	200	-	-	ms
T_7	0.5	-	10	ms

Note)
1. Do not insert the mating cable when system turn on.
2. Valid Data have to meet "3-3. LVDS Signal Timing Specifications"
3. LGD recommend the rising sequence of LED after the Vcc and valid status of LVDS turn on.

※ LGD recommend below sequence of LED Driver inputs.

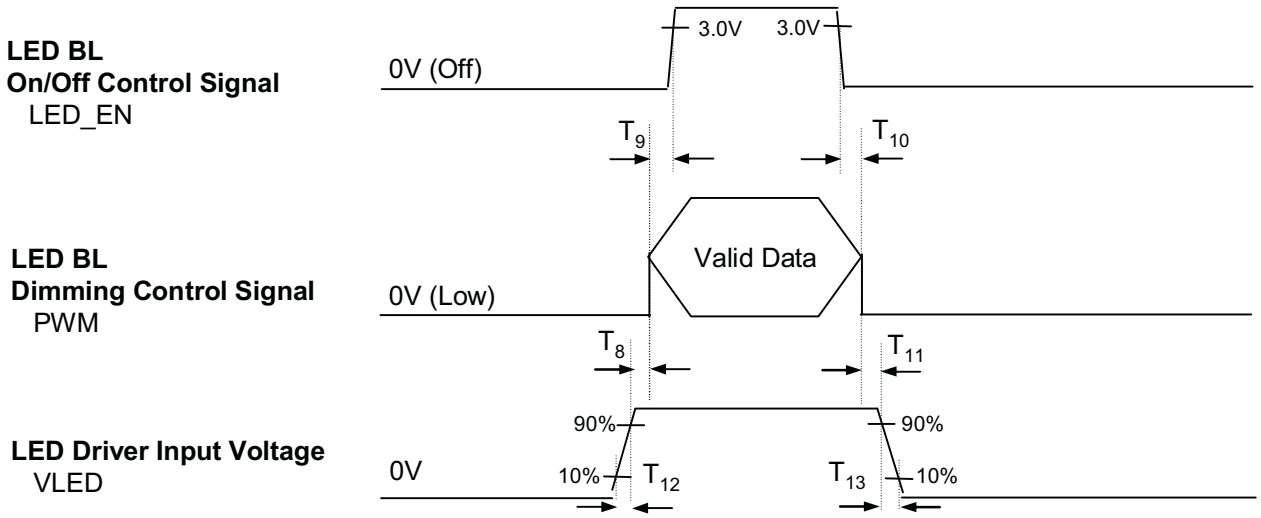


Table 6-1. POWER SEQUENCE TABLE

LED Parameter	Value			Units
	Min.	Typ.	Max.	
T_8	10	-	-	ms
T_9	0	-	-	ms
T_{10}	0	-	-	ms
T_{11}	10	-	-	ms
T_{12}	0.5	-	-	ms
T_{13}	0	-	5000	ms

Note)
1. LVDS, LED_EN and PWM need to be on pull-down condition on invalid status.

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 20 minutes in a dark environment at 25°C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and Θ equal to 0°.
FIG. 1 presents additional information concerning the measurement equipment and method.

FIG. 1 Optical Characteristic Measurement Equipment and Method

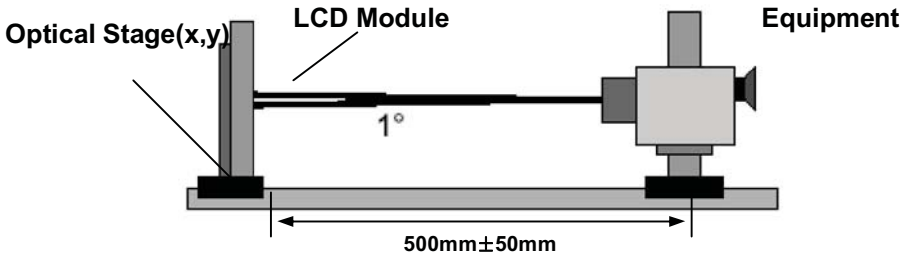


Table 7. OPTICAL CHARACTERISTICS

Ta=25°C, VCC=3.3V, fv=60Hz, f_{CLK}= 70.0MHz,
Backlight : LGD Standard

Parameter	Symbol	Values			Units	Notes
		Min	Typ	Max		
Transmittance (With POL)	%	-	6.1%			
Surface Luminance, white	L_{WH}	170	200			
Contrast Ratio	CR	400	500	-		1
Response Time	$Tr_{R+}Tr_D$	-	16	25	ms	2
Color Coordinates						
RED	RX	0.556	0.586	0.616		
	RY	0.317	0.347	0.377		
GREEN	GX	0.311	0.341	0.371		
	GY	0.528	0.558	0.588		
BLUE	BX	0.127	0.157	0.187		
	BY	0.087	0.117	0.147		
WHITE	WX	0.283	0.313	0.343		
	WY	0.299	0.329	0.359		
Viewing Angle						3
x axis, right(Φ=0°)	Θr	40	45	-	degree	
x axis, left (Φ=180°)	Θl	40	45	-	degree	
y axis, up (Φ=90°)	Θu	10	15	-	degree	
y axis, down (Φ=270°)	Θd	30	35	-	degree	
Gray Scale						4
Color Gamut	C/G	-	45	-	%	

※ It can be guaranteed only when B/L have sheets that LGD recommended. (Prism & Diffuser sheet)

Note)

1. Contrast Ratio(CR) is defined mathematically as

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

2. Response time is the time required for the display to transition from white to black (rise time, TrR) and from black to white(Decay Time, TrD). For additional information see FIG 2.

3. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 3.

4. Gray scale specification * fV = 60Hz

Gray Level	Luminance [%] (Typ)
L0	0.2
L7	1.2
L15	4.8
L23	10.9
L31	21.0
L39	34.8
L47	52.5
L55	74.2
L63	100.0

FIG. 2 Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”.

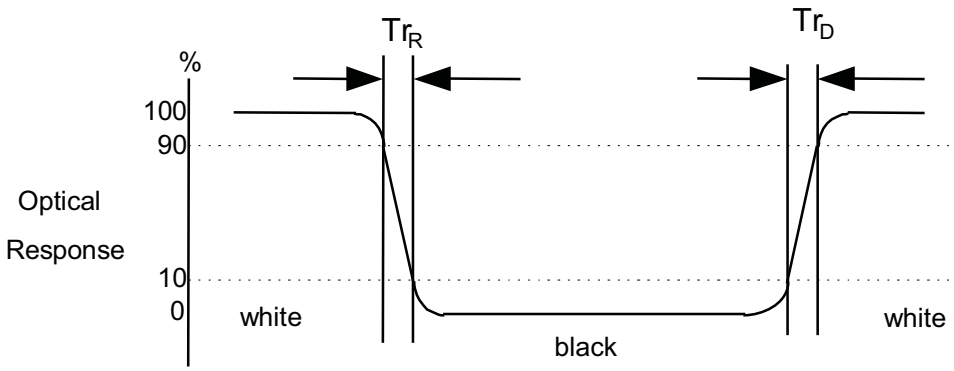
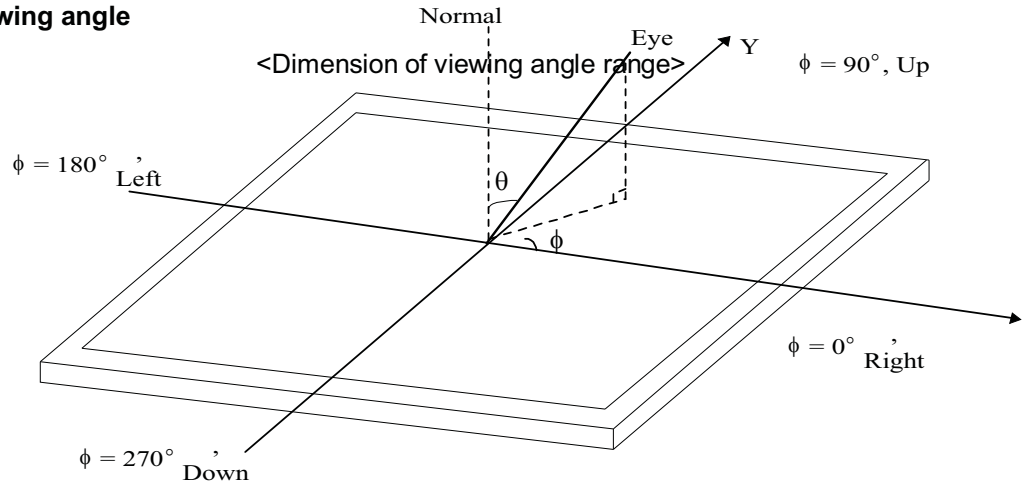


FIG. 3 Viewing angle



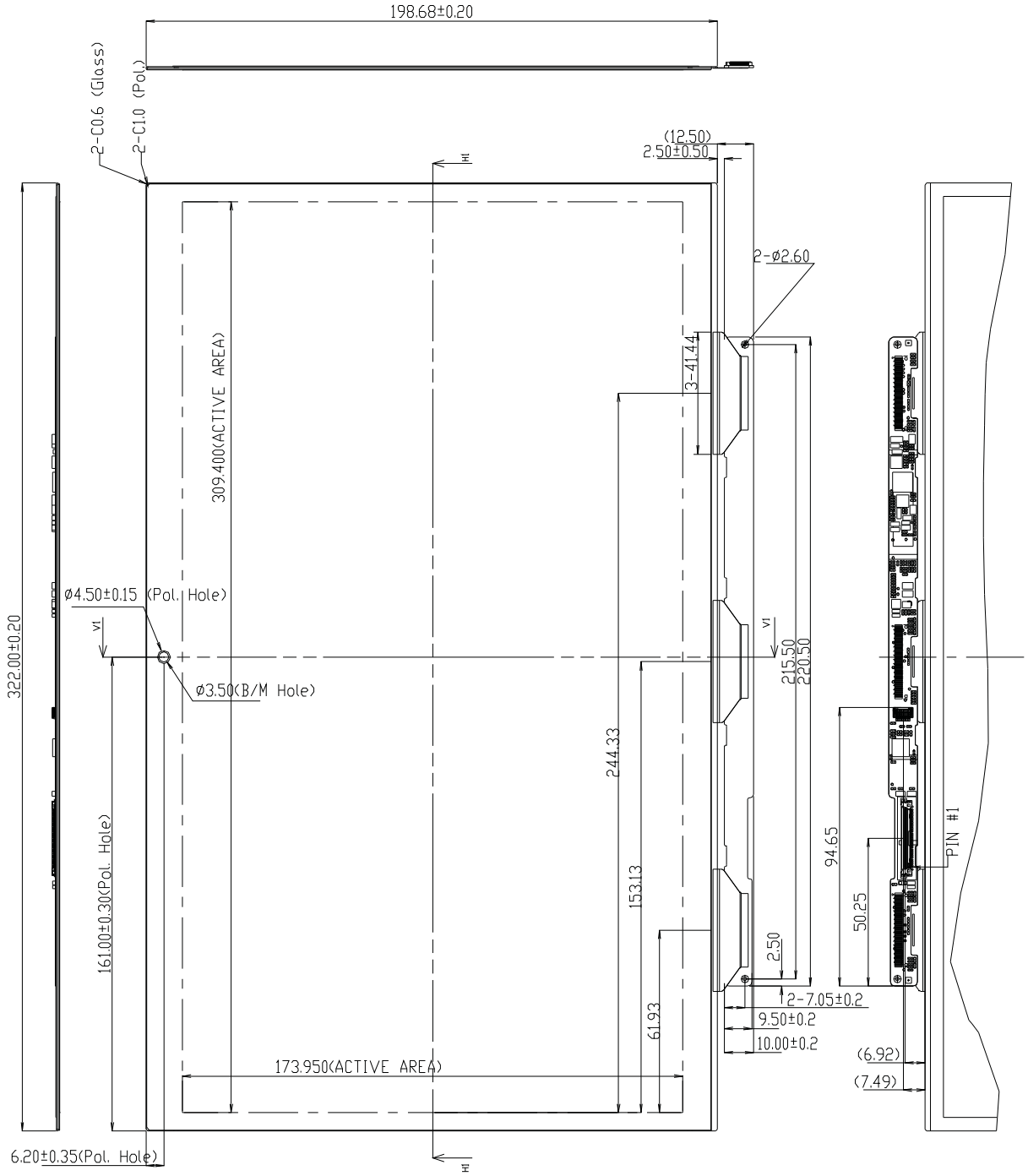
5. Mechanical Characteristics

The contents provide general mechanical characteristics for the model LP140WH6. In addition the figures in the next page are detailed mechanical drawing of the Board Ass'y.

Outline Dimension (Without PCB)	Horizontal (A)	322 ± 0.2mm
	Vertical (B)	198.68 ± 0.2mm
	Thickness	1.27mm (Typ.)
Active Display Area	Horizontal	309.40 mm
	Vertical	173.95 mm
Weight	190 g (Max.)	
Surface Treatment	Hard Coating(3H), Glare treatment of the front polarizer	

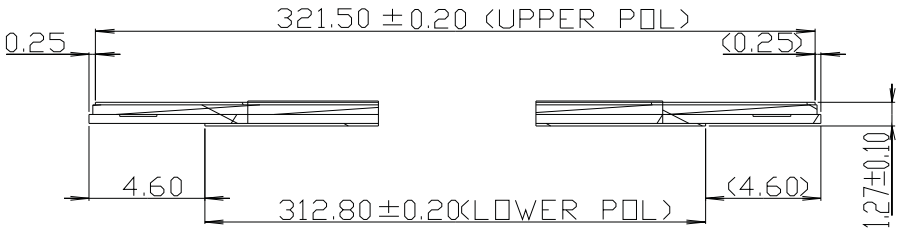
<FRONT VIEW>

Note) Unit:[mm], General tolerance: ± 0.5mm

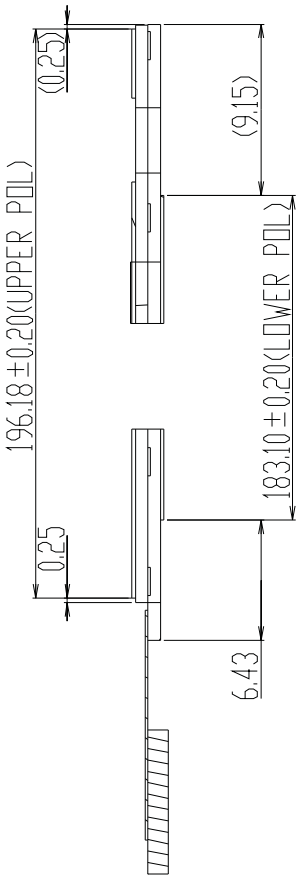


<SECTION VIEW>

Note) Unit:[mm], General tolerance: ± 0.25mm



SECTION H1-H1



SECTION V1-V1

6. Reliability

Environment test condition

No.	Test Item	Conditions
1	High temperature storage test	Ta= 60°C, 240h
2	Low temperature storage test	Ta= -20°C, 240h
3	High temperature operation test	Ta= 50°C, 50%RH, 240h
4	Low temperature operation test	Ta= 0°C, 240h
5	Altitude operating storage / shipment	0 ~ 10,000 feet (3,048m) 24Hr 0 ~ 40,000 feet (12,192m) 24Hr

{ Result Evaluation Criteria }
There should be no change which might affect the practical display function when the display quality test is conducted under normal operating condition.

7. International Standards

7-1. Environment

a) RoHS, Directive 2002/95/EC of the European Parliament and of the council of 27 January 2003

8. Packing

8-1. Designation of Lot Mark

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)
E : MONTH

D : YEAR
F ~ M : SERIAL NO.

Note

1. YEAR

Year	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Mark	A	B	C	D	E	F	G	H	J	K

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial No. is printed on the label. The label is attached to the backside of the LCD module.
This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one box : 20pcs

b) Box Size : 445 mm X 373 mm X 165 mm

9. PRECAUTIONS

Please pay attention to the followings when you use this Board ass'y.

9-1. Assembly PRECAUTIONS

(1) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(2) You should adopt radiation structure to satisfy the temperature specification.
(3) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(4) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(5) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(6) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(7) Do not open the case because inside circuits do not have sufficient strength.
(8) Mechanical structure for backlight system should be designed for sustaining board ass'y safely.

9-2. OPERATING PRECAUTIONS

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=± 200mV(Over and under shoot voltage)

(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
(7) Please do not give any mechanical and/or electrical impact to board assy. Otherwise, it can't be operated its full characteristics perfectly.

9-3. ELECTROSTATIC DISCHARGE CONTROL

Board ass'y is composed of electronic circuits, so it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch drive IC directly.
Panel ground path should be connected to metal ground.

9-4. PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

9-5. STORAGE

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

9-6. HANDLING PRECAUTIONS FOR PROTECTION FILM

(1) When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt to remain on the polarizer.
Please carefully peel off the protection film without rubbing it against the polarizer.
(3) When the Board ass'y with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
(4) You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

10. Inspection-Free Area

❑LGD define Inspection-Free Area as 0.7mm between
- Polarizer edge to glass edge area (assigned to all side of panel)
- Web-cam hole area

❑LGD does not guarantee the Web-Cam hole contamination caused by the finger touch after shipping out.

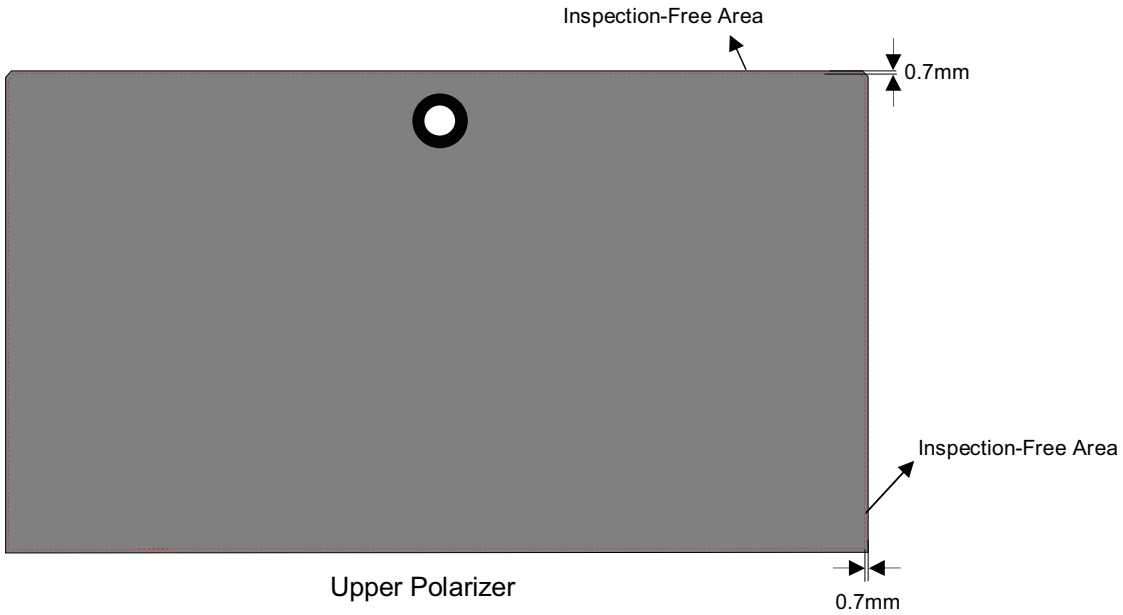


Fig 1. Defining Upper Polarizer area

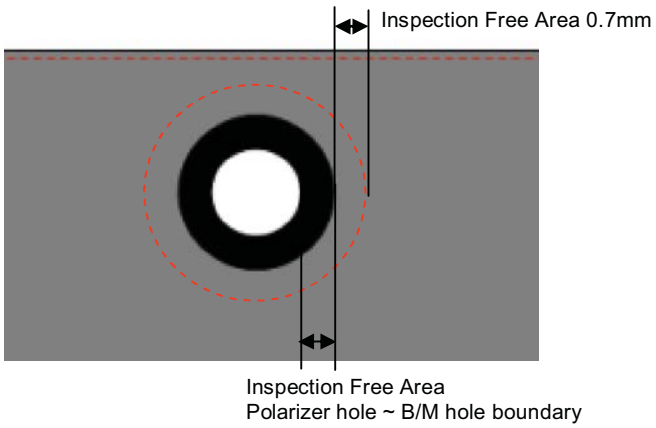


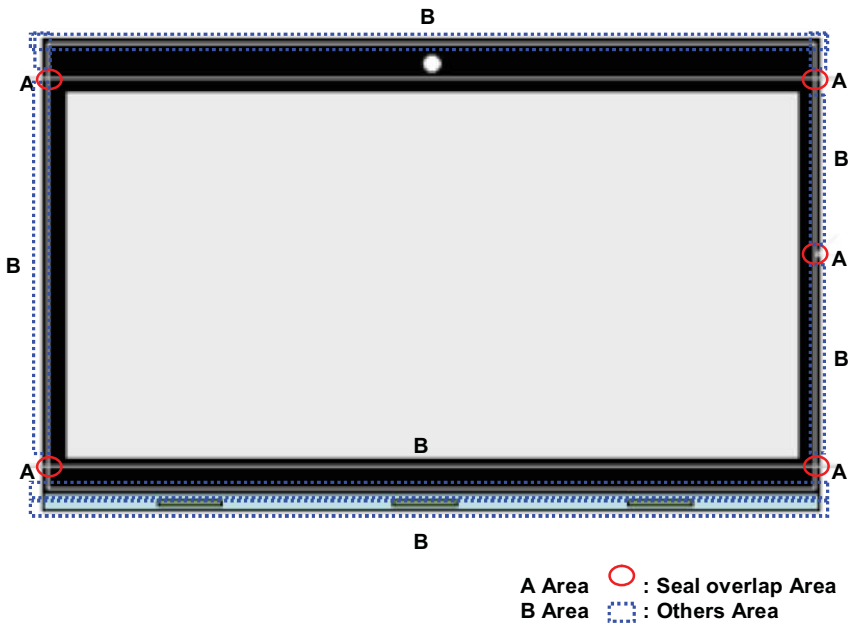
Fig 2. Defining Webcam Hole area

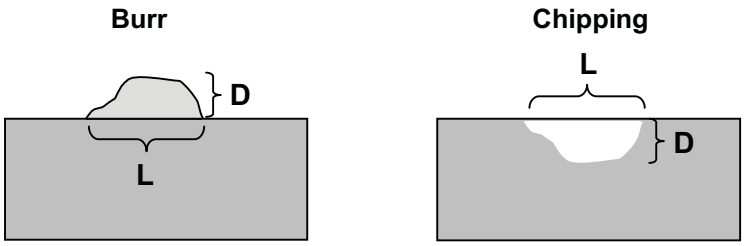
11. Panel Burr & Chip (1)

❑LGD define specification of chipping and remained bur based on the LGD capability data

<Standard Line : TFT, unit : mm>

Model	Edge			
	Seal Cross (A)		Others (B)	
	Burr	Chipping	Burr	Chipping
LP140WH6-TJA1 LP140WH6-TJB1 LP156WH8-TJA1	L ≤ 4.0 D ≤ 0.5	L ≤ 4.0 D ≤ 1.0	L ≤ 4.0 D ≤ 0.4	L ≤ 4.0 D ≤ 1.0

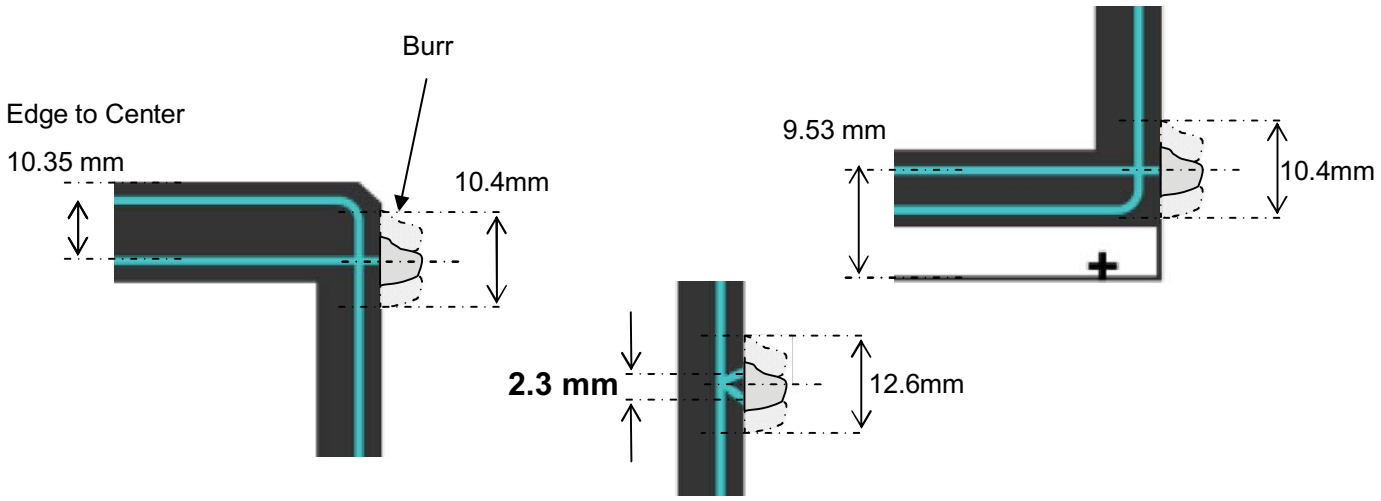




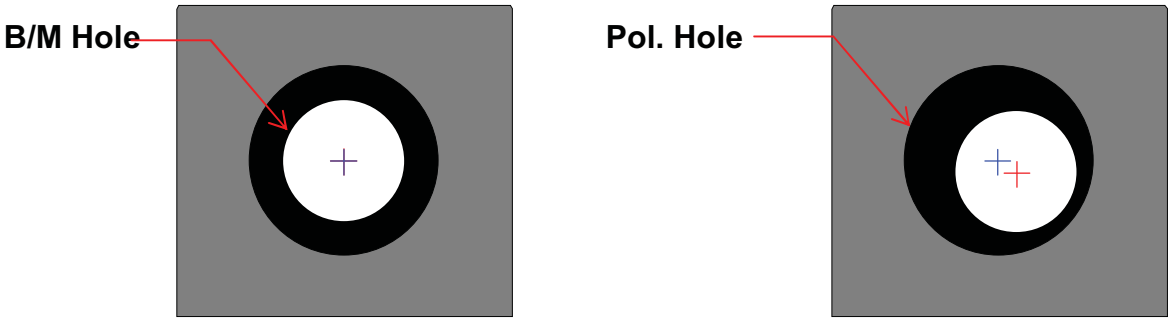
11. Panel Burr & Chip (2)

❑LGD define specification of chipping and remained bur based on the LGD capability data

Burr position in "A" area's



12. Web-Cam Hole Shift



[OK Sample] [NG Sample]

X-Direction Shift : ±0.25mm

Y-Direction Shift : ±0.30mm

APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 1/3

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
Header	0	00	Header	00	00000000
	1	01	Header	FF	11111111
	2	02	Header	FF	11111111
	3	03	Header	FF	11111111
	4	04	Header	FF	11111111
	5	05	Header	FF	11111111
	6	06	Header	FF	11111111
	7	07	Header	00	00000000
Vendor / Product EDID Version	8	08	EISA manufacture code (3 Character ID) LGD	30	00110000
	9	09	EISA manufacture code (Compressed ASCII)	E4	11100100
	10	0A	Panel Supplier Reserved - Product Code 02F9h	F9	11111001
	11	0B	(Hex. LSB first)	02	00000010
	12	0C	LCD Module Serial No - Preferred but Optional ("0" If not used)	00	00000000
	13	0D	LCD Module Serial No - Preferred but Optional ("0" If not used)	00	00000000
	14	0E	LCD Module Serial No - Preferred but Optional ("0" If not used)	00	00000000
	15	0F	LCD Module Serial No - Preferred but Optional ("0" If not used)	00	00000000
	16	10	Week of Manufacture 00 weeks	00	00000000
	17	11	Year of Manufacture 2011 years	15	00010101
	18	12	EDID structure version # = 1	01	00000001
	19	13	EDID revision # = 3	03	00000011
Display Parameters	20	14	Video input Definition = Digital signal	80	10000000
	21	15	Max H image size (Rounded cm) = 31 cm	1F	00011111
	22	16	Max V image size (Rounded cm) = 17 cm	11	00010001
	23	17	Display gamma = (gamma*100)-100 = Example:(2.2*100)-100=120 = 2.2 Gamma	78	01111000
	24	18	Feature Support (no_DPMS, no_Active Off/Very Low Power, RGB color display, Timing BLK 1,no GTF)	0A	00001010
Panel Color Coordinates	25	19	Red/Green Low Bits (RxRy/GxGy)	37	00110111
	26	1A	Blue/White Low Bits (BxBy/WxWy)	45	01000101
	27	1B	Red X Rx = 0.586	96	10010110
	28	1C	Red Y Ry = 0.347	58	01011000
	29	1D	Green X Gx = 0.341	57	01010111
	30	1E	Green Y Gy = 0.558	8E	10001110
	31	1F	Blue X Bx = 0.157	28	00101000
	32	20	Blue Y By = 0.117	1E	00011110
	33	21	White X Wx = 0.313	50	01010000
	34	22	White Y Wy = 0.329	54	01010100
Established Timings	35	23	Established timing 1 (00h if not used)	00	00000000
	36	24	Established timing 2 (00h if not used)	00	00000000
	37	25	Manufacturer's timings (00h if not used)	00	00000000
Standard Timing ID	38	26	Standard timing ID1 (01h if not used)	01	00000001
	39	27	Standard timing ID1 (01h if not used)	01	00000001
	40	28	Standard timing ID2 (01h if not used)	01	00000001
	41	29	Standard timing ID2 (01h if not used)	01	00000001
	42	2A	Standard timing ID3 (01h if not used)	01	00000001
	43	2B	Standard timing ID3 (01h if not used)	01	00000001
	44	2C	Standard timing ID4 (01h if not used)	01	00000001
	45	2D	Standard timing ID4 (01h if not used)	01	00000001
	46	2E	Standard timing ID5 (01h if not used)	01	00000001
	47	2F	Standard timing ID5 (01h if not used)	01	00000001
	48	30	Standard timing ID6 (01h if not used)	01	00000001
	49	31	Standard timing ID6 (01h if not used)	01	00000001
	50	32	Standard timing ID7 (01h if not used)	01	00000001
	51	33	Standard timing ID7 (01h if not used)	01	00000001
	52	34	Standard timing ID8 (01h if not used)	01	00000001
	53	35	Standard timing ID8 (01h if not used)	01	00000001

APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 2/3

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
Timing Descriptor #1	54	36	Pixel Clock/10,000 (LSB) 70 MHz @ 60Hz	58	01011000
	55	37	Pixel Clock/10,000 (MSB)	1B	00011011
	56	38	Horizontal Active (lower 8 bits) 1366 Pixels	56	01010110
	57	39	Horizontal Blanking(Thp-HA) (lower 8 bits) 126 Pixels	7E	01111110
	58	3A	Horizontal Active / Horizontal Blanking(Thp-HA) (upper 4:4bits)	50	01010000
	59	3B	Vertical Avtive 768 Lines	00	00000000
	60	3C	Vertical Blanking (Tvp-HA) (DE Blanking typ.for DE only panels) 14 Lines	0E	00001110
	61	3D	Vertical Active : Vertical Blanking (Tvp-HA) (upper 4:4bits)	30	00110000
	62	3E	Horizontal Sync. Offset (Thfp) 36 Pixels	24	00100100
	63	3F	Horizontal Sync Pulse Width (HSPW) 48 Pixels	30	00110000
	64	40	Vertical Sync Offset(Tvfp) : Sync Width (VSPW) 3 Lines : 5 Lines	35	00110101
	65	41	Horizontal Vertical Sync Offset/Width (upper 2bits)	00	00000000
	66	42	Horizontal Image Size (mm) 310 mm	36	00110110
	67	43	Vertical Image Size (mm) 174 mm	AE	10101110
	68	44	Horizontal Image Size / Vertical Image Size	10	00010000
	69	45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000
	70	46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000
	71	47	Non-Interlace, Normal display, no stereo, Digital Separate (Vsync_NEG, Hsync_NEG), DE only note : LSB is set to '1' if panel is DE-timing only. H/V can be ignored.	19	00011001
Timing Descriptor #2	72	48	Flag	00	00000000
	73	49	Flag	00	00000000
	74	4A	Flag	00	00000000
	75	4B	Data Type Tag (Descriptor Defined by manufacturer)	00	00000000
	76	4C	Flag	00	00000000
	77	4D	Descriptor Defined by manufacturer	00	00000000
	78	4E	Descriptor Defined by manufacturer	00	00000000
	79	4F	Descriptor Defined by manufacturer	00	00000000
	80	50	Descriptor Defined by manufacturer	00	00000000
	81	51	Descriptor Defined by manufacturer	00	00000000
	82	52	Descriptor Defined by manufacturer	00	00000000
	83	53	Descriptor Defined by manufacturer	00	00000000
	84	54	Descriptor Defined by manufacturer	00	00000000
	85	55	Descriptor Defined by manufacturer	00	00000000
	86	56	Descriptor Defined by manufacturer	00	00000000
	87	57	Descriptor Defined by manufacturer	00	00000000
	88	58	Descriptor Defined by manufacturer	00	00000000
	89	59	Descriptor Defined by manufacturer	00	00000000
Timing Descriptor #3	90	5A	Flag	00	00000000
	91	5B	Flag	00	00000000
	92	5C	Flag	00	00000000
	93	5D	Data Type Tag (ASCII String)	FE	11111110
	94	5E	Flag	00	00000000
	95	5F	ASCII String L	4C	01001100
	96	60	ASCII String G	47	01000111
	97	61	ASCII String	20	00100000
	98	62	ASCII String D	44	01000100
	99	63	ASCII String i	69	01101001
	100	64	ASCII String s	73	01110011
	101	65	ASCII String p	70	01110000
	102	66	ASCII String l	6C	01101100
	103	67	ASCII String a	61	01100001
	104	68	ASCII String y	79	01111001
	105	69	Manufacturer P/N(If<13 char--> 0Ah, then terminate with ASCII code 0Ah,set remaining char = 2	0A	00001010
	106	6A	Manufacturer P/N(If<13 char--> 0Ah, then terminate with ASCII code 0Ah,set remaining char = 2	20	00100000
	107	6B	Manufacturer P/N(If<13 char--> 0Ah, then terminate with ASCII code 0Ah,set remaining char = 2	20	00100000

APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 3/3

	Byte (Dec)	Byte (Hex)	Field Name and Comments		Value (Hex)	Value (Bin)
Timing Descriptor #4	108	6C	Flag		00	00000000
	109	6D	Flag		00	00000000
	110	6E	Flag		00	00000000
	111	6F	Data Type Tag (ASCII String)		FE	11111110
	112	70	Flag		00	00000000
	113	71	ASCII String	L	4C	01001100
	114	72	ASCII String	P	50	01010000
	115	73	ASCII String	1	31	00110001
	116	74	ASCII String	4	34	00110100
	117	75	ASCII String	0	30	00110000
	118	76	ASCII String	W	57	01010111
	119	77	ASCII String	H	48	01001000
	120	78	ASCII String	6	36	00110110
	121	79	ASCII String	-	2D	00101101
	122	7A	ASCII String	T	54	01010100
	123	7B	ASCII String	J	4A	01001010
	124	7C	ASCII String	A	41	01000001
	125	7D	ASCII String	1	31	00110001
Checksum	126	7E	Extension flag (# of optional 128 panel ID extension block to follow, Typ = 0)		00	00000000
	127	7F	Check Sum (The 1-byte sum of all 128 bytes in this panel ID block shall = 0)		E6	11100110